

Application No.: 10/626025

Docket No.: 34650-00179USC2

**AMENDMENTS TO THE CLAIMS**

1-37. (CANCEL)

38. (NEW) A radio for transmitting and receiving, via an antenna, of a plurality of high-frequency signals in a time-division-duplex mode on a single IC chip, the radio comprising:  
a circuit path adapted to connect the antenna to a data output port and to a data input port, wherein the circuit path comprises:

- (1) a down-conversion section for down-converting received high-frequency signals of the plurality of high-frequency signals;
- (2) a bandpass filter for filtering signals derived from the received high-frequency signals;
- (3) a detector for detecting a received data signal from a received filtered signal, wherein the received data signal is sent to the data output port; and
- (4) an up-conversion section for up-converting an information signal received from the data input port to a high-frequency signal of the plurality of high-frequency signals; wherein the circuit path comprising the bandpass filter, the detector, the up-conversion section, and the down-conversion section is integrated into the single IC chip; and wherein bandpass filtering operations are performed by components integrated into the single IC chip.

39. (NEW) The radio of claim 38, wherein the up-conversion section comprises a variable controlled oscillator.

40. (NEW) The radio of claim 38, wherein the up-conversion section comprises a directly modulated variable controlled oscillator.

41. (NEW) The radio of claim 38, wherein the radio comprises an image-rejection-mixer stage.

42. (NEW) The radio of claim 38, further comprising automatic re-transmission request error correction means for data transfer.

43. (NEW) The radio of claim 38, further comprising autotuning means for autotuning a plurality of filters and the detector.

44. (NEW) The radio of claim 38, further comprising a digital power-down control circuit to provide power-down control for the radio, wherein the power-down control circuit is integrated into the single IC chip.

45. (NEW) The radio of claim 38, further comprising a low-power oscillator integrated into the single IC chip.

46. (NEW) The radio of claim 38, wherein the signal derived from received high-frequency signals of the plurality of high-frequency signals is a low intermediate frequency signal.

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47. (NEW) The radio of claim 38, wherein the circuit path further comprises a low-pass filter for filtering the received data signal output by the detector and the low-pass filter is connected to the detector and the data output port.

48. (NEW) The radio of claim 38, further comprising the antenna.

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49. (NEW) A method for communication of at least one data signal, wherein all of the steps for the method of communication are performed on a single IC chip, the method comprising the steps of:

receiving a first high-frequency information signal transmitted over an RF link in a time-division-duplex mode;

converting the received first high-frequency information signal into a low-intermediate-frequency signal using a single variable controlled oscillator;

filtering the low-intermediate-frequency signal using a bandpass filter;

detecting a received data signal using a detector;

sending the detected received data signal from the detector to a data output port;

converting a data signal to a second high-frequency information signal using the single variable controlled oscillator, and

transmitting the second high-frequency information signal over the RF link.

50. (NEW) The method of claim 49, wherein the low-intermediate-frequency signal is centered at about 3 MHz.

51. (NEW) The method of claim 49, wherein converting the received first high-frequency information signal uses an image-rejection-mixer circuit.

52. (NEW) The method of claim 49, wherein resonators are implemented for the single variable controlled oscillator without components external to the single IC chip.

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53. (NEW) A radio for transmitting and receiving, via an antenna, of a plurality of high-frequency signals in a time-division-duplex mode on a single IC chip, the radio comprising: a circuit path adapted to connect the antenna to a data output port and to a data input port, wherein the circuit path comprises:

(1) a bandpass filter for filtering signals derived from the received high-frequency signals;

(2) a detector for detecting a received data signal from a received filtered signal, wherein the received data signal is sent to the data output port; and

(3) an up-conversion section for up-converting an information signal received from the data input port to a high-frequency signal of the plurality of high-frequency signals;

(4) a shaping filter connected to an input of the up-conversion section; wherein the circuit path comprising the bandpass filter, the detector, the up-conversion section, and the shaping filter is integrated into the single IC chip; and wherein bandpass filtering operations are performed by components integrated into the single IC chip.

54. (NEW) The radio of claim 53, wherein the up-conversion section comprises a variable controlled oscillator.

55. (NEW) The radio of claim 53, wherein the up-conversion section comprises a directly modulated variable controlled oscillator.

56. (NEW) The radio of claim 53, wherein the radio comprises an image-rejection-mixer stage.

57. (NEW) The radio of claim 53, further comprising automatic re-transmission request error correction means for data transfer.

58. (NEW) The radio of claim 53, further comprising autotuning means for autotuning a plurality of filters and the detector.

59. (NEW) The radio of claim 53, further comprising a digital power-down control circuit to provide power-down control for the radio, wherein the power-down control circuit is integrated into the single IC chip.

60. (NEW) The radio of claim 53, further comprising a low-power oscillator integrated into the single IC chip.

61. (NEW) The radio of claim 53, wherein the signal derived from received high-frequency signals of the plurality of high-frequency signals is a low intermediate frequency signal.

62. (NEW) The radio of claim 53, wherein the circuit path further comprises a low-pass filter for filtering the received data signal output by the detector and the low-pass filter is connected to the detector and the data output port.

63. (NEW) The radio of claim 53, further comprising the antenna.